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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Y. NUNOGAWA et al

Serial No. 09/555,010 Group Art Unit: 2682

Filed: May 23, 2000

For: HIGH FREQUENCY POWER AMPLIFYING CIRCUIT, AND MOBILE COMMUNICATION APPARATUS USING IT

REQUEST FOR DECLARATION OF AN INTERFERENCE IN ACCORDANCE WITH 37 CFR §1.607

Commissioner for Patents
Washington, D.C. 20231

Sir:

It is respectfully requested that an Interference be declared between the present application and U.S. Patent Nos. 6,307,364 B1 (the '364 patent) and 6,329,809 B1 (the '809 patent), which are commonly assigned. Pursuant to 37 CFR §1.607(b), examination of the present application should be conducted with special dispatch.

The present application has a filing date of May 23, 2000, with a PCT International Filing Date of November 28, 1997. The '364 patent issued on October 23, 2001 from application Serial No. 09/384,679 having a U.S. filing date of August 27, 1999. The '809 patent issued on December 11, 2001 from application Serial No. 09/492,488 having a U.S. filing

date of January 27, 2000 and was filed as a continuation-in-part of application Serial No. 09/384,679.

Claims from each of these patents have been copied as set forth in the remarks contained in an amendment accompanying this request. In particular, claims 1-4, 9-11, 13 and 14 of the '364 patent have been copied as claims 26-29, 34-36, 41 and 42 of the present application other than claim numbering. The word "step" in claim 14 of the '364 has been changed to "claim" in claim 42 of the present application. Claim 10 of the '809 patent has been copied as claim 44 of the present application. The subject matter of claims 6 and 7 of the '364 patent have been copied as claims 31 and 32 in the present application. The subject matter of claim 16 of the '809 patent has been copied as claim 45 of the present application.

PROPOSED COUNT

Applicants propose the following Count as the Proposed Count for the Interference:

Proposed Count for the Interference

An apparatus comprising:

a first transistor to receive and amplify an RF signal and output a first signal;

a second transistor to receive and amplify the RF signal, wherein the second transistor is physically smaller than the first transistor; and

a circuit to receive an RF signal amplified by the second transistor and to output a second signal proportional to the first signal.

Claim 16 of the present application is identical to this Proposed Count for the Interference. All of the claims in the '364 patent and the '809 patent correspond to this proposed count. The proposed count is of a broader scope than claim 1 of the '364 patent and is patentable over the prior art cited in the '364 patent and the '809 patent as well as additional art submitted in an accompanying Information Disclosure Statement.

35 U.S.C. §135(b)

New claims 16-49 of the present application have been presented by amendment on October 23, 2002, which is not more than one year from the issuance of the '364 and '809 patents.

EFFECTIVE FILING DATE

The present application has an International Filing Date of November 28, 1997, which in accordance with 35 U.S.C. §363 may be considered the effective U.S. filing date thereof. A verified English language translation of the international application has already been filed. Since the effective U.S. filing date of the present application is November 28, 1997, which is more than twenty (20) months prior to the effective U.S. filing dates of the '364 and '809 patents, it is requested that the Interference be declared between the present application and the '364 and '809 patents, with the Applicants of the present application being designated as the Senior Party.

37 CFR §1.607(a)(5)

Pursuant to 37 CFR §1.607(a)(5) the terms of the claims added by the accompanying amendment, including those claims copied from the '364 and '809 patents, have been applied to the disclosure of the present application in the attached Claim Support Chart.

CONCLUSION

A declaration of the requested Interference is respectfully requested. The Examiner is hereby invited to contact the undersigned by telephone with any questions. The Commissioner is hereby authorized to charge Deposit Account No. 50-1417 for any fees that are deemed necessary.

Respectfully submitted,

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CLAIM SUPPORT CHART

PENDING CLAIMS	CORRESPONDING SUPPORT IN U.S. SERIAL NO.09/555,010
16. An apparatus comprising:	(Fig. 1; pg 1, lines 2-8; and pg. 2, lines 9-14)
a first transistor to receive and amplify an RF signal and output a first signal;	T1 (Figs. 7 and 11; pg. 6, lines 10-12, pg. 20, lines 6-21)
a second transistor to receive and amplify the RF signal, wherein the second transistor is physically smaller than the first transistor; and	T2 (Figs. 7 and 11; and spec. pg. 2, line 23 - pg. 3, line 7; pg. 6, lines 16-19; pg. 10, lines 11-14; pg. 16, line 24 to pg. 17, line 13; pg. 20, lines 6-21; pg. 22, line 28 to pg. 23 line 12; pg. 25, lines 8-14; and original claim 1)
a circuit to receive an RF signal amplified by the second transistor and to output a second signal proportional to the first signal.	Rs1, (Fig. 11; pg. 2, line 27 - pg. 3, line 5; pg. 16 lines 11-14; pg. 17, lines 5-9; pg. 20, lines 15-21) Rs (Fig. 7)
17. The apparatus of claim 16, wherein the circuit comprises a resistor element.	Rs1, (Fig. 11; pg. 2, line 27 - pg. 3, line 5; pg. 16 lines 11-14; pg. 17, lines 5-9; pg. 20, lines 15-21) Rs (Fig. 7)
18. The apparatus of claim 16, further comprising a bias network to establish an operating point for the first transistor.	R1 (Fig. 11) R1 & R2 (Fig. 7) Numerals (4), (5), (8-1)-(8-N) (Fig. 1) (pg. 6, lines 4-7 and 23-27; and pg. 20, lines 6-21)
19. The apparatus of claim 18, wherein the bias network is configured to establish an operating point for the second transistor.	(Figs. 7 and 11 and pg. 9 lines 12-16; pg. 10, lines 8-14; and pg. 14 line 27 to pg. 15, line 9)

20. The apparatus of claim 16, wherein said circuit generates a sense voltage proportional to power of said first transistor.	(Figs. 7 and 11; and pg. 2, line 27 to pg. 3, line 5; pg. 16, lines 11-14 and pg 20 lines 15-21)
21. The apparatus of claim 16, wherein said first transistor comprises a first field-effect transistor, and said second transistor comprises a second field-effect transistor.	T1 (Figs. 7 and 11; and pg. 20, lines 6-21) T2 (Figs. 7 and 11; and pg. 10, lines 11-14; pg. 16, line 24 to pg. 17, line 13; pg. 20, lines 6-21; pg. 22, line 28 to pg. 23 line 12; and original claim 12)
22. The apparatus of claim 21, wherein said first signal corresponds to a drain output of said first field-effect transistor, and said second signal corresponds to a drain output of said second field-effect transistor.	(pg. 17, lines 5-9; pg. 20 lines 15-21)
23. The apparatus of claim 22, wherein said circuit comprises a resistor element coupled to a drain of said second field-effect transistor.	Rs1 (Fig. 11) Rs (Fig. 7)
24. The apparatus of claim 23, wherein a gate of said first field-effect transistor is coupled to a gate of said second field-effect transistor.	T1, T2 (Fig. 11)
25. The apparatus of claim 24, wherein said RF signal is applied to said gate of said first field-effect transistor and is applied to said gate of said second field-effect transistor.	Pin, T1, T2 (Fig. 11)

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26. A system for sensing RF amplifier output power comprising:	(Fig. 1; pg 1, lines 2-8; and pg. 2, lines 9-14)
a RF amplifier transistor configured to receive and amplify a RF signal;	T1 (Figs. 7 and 11; pg. 6, lines 10-12, pg. 20, lines 6-21)
a sampling transistor configured to receive and amplify a RF signal, wherein the sampling transistor is physically smaller than the RF amplifier transistor such that the sampling transistor is capable of producing a proportionally smaller amplified RF signal than that capable of being produced by the RF amplifier transistor for a RF input signal common to both the RF amplifier transistor and the sampling transistor; and	T2 (Figs. 7 and 11; and spec. pg. 2, line 23 - pg. 3, line 7; pg. 6, lines 16-19; pg. 10, lines 11-14; pg. 16, line 24 to pg. 17, line 13; pg. 20, lines 6-21; pg. 22, line 28 to pg. 23 line 12; pg. 25, lines 8-14; and original claim 1)
a current sensing circuit configured to receive a RF signal amplified by the sampling transistor and generate a current proportional to a RF signal amplified by the RF amplifier transistor.	Circuitry generates a current (DRAIN (2)) that is proportional to the current of T1 (DRAIN (1)) (Figs. 7 and 11, pg. 16, line 24 to pg. 17, line 9; and pg. 20, lines 6-21)
27. The system according to claim 26, further including a bias network configured to establish a quiescent operating point for the RF amplifier transistor.	R1 (Fig. 11) R1 & R2 (Fig. 7) Numerals (4), (5), (8-1)-(8-N) (Fig. 1; pg. 6, lines 4-7 and 23-27; and pg. 20, lines 6-21)
28. The system according to claim 27, wherein the bias network is further configured to establish a quiescent operating point for the sampling transistor, by associating a first bias resistor with the sampling transistor.	R1 (Fig. 11) R2 (Fig. 7)
29. The system according to claim 28, wherein the bias network comprises a second bias resistor associated with the RF amplifier transistor.	R1 (Fig. 11) R1 (Fig. 7)
30. The system according to claim 28, wherein said first bias resistor and said second bias resistor are the same resistor.	R1 (Fig. 11)

31. The system according to claim 26, further comprising a first RF signal coupling capacitor configured to pass the RF signal to the RF amplifier transistor.	C1 (Figs. 7 and 11)
32. The system according to claim 31, further comprising a second RF signal coupling capacitor configured to pass the RF signal to the sampling transistor.	C1 (Fig. 11)
33. The system according to claim 32, wherein said first RF signal coupling capacitor and the second RF signal coupling capacitor are the same capacitor.	C1 (Fig. 11)
34. A system for sensing RF amplifier output power comprising:	(Fig. 1; pg 1, lines 2-8; and pg. 2, lines 9-14)
means for amplifying a RF input signal and generating a RF output signal therefrom;	T1 (Figs. 7 and 11; pg. 6, lines 10-12, pg. 20, lines 6-21)
means for sampling a RF input signal that is associated with both the amplifying means and the sampling means and generating a sampled signal therefrom; and	T2 (Figs. 7 and 11; and spec. pg. 2, line 23 - pg. 3, line 7; pg. 6, lines 16-19; pg. 10, lines 11-14; pg. 16, line 24 to pg. 17, line 13; pg. 20, lines 6-21; pg. 22, line 28 to pg. 23 line 12; pg. 25, lines 8-14; and original claim 1)
means for sensing the sampled signal and generating a current sensing signal therefrom proportional to a power amplitude associated with the RF output signal.	Circuitry generates a current (DRAIN (2)) that is proportional to the current of T1 (DRAIN (1)) (Figs. 7 and 11, pg. 16, line 24 to pg. 17, line 9; and pg. 20, lines 6-21)
35. The system according to claim 34, further comprising biasing means for biasing the sampling means and further for biasing the amplifying means such that a bias current associated with the sampling means is proportional to a bias current associated with the amplifying means.	R1 (Fig. 11) R1 & R2 (Fig. 7) Numerals (4), (5), (8-1)-(8-N) (Fig. 1; pg. 6, lines 4-7 and 23-27; and pg. 20, lines 6-21)
36. The system according to claim 35, wherein the amplifying means comprises a first transistor.	T1 (Figs. 7 and 11; pg. 6, lines 10-12, pg. 20, lines 6-21)

37. The system according to claim 36, wherein said means for sampling comprises a second transistor, and said second transistor is physically smaller than said first transistor.	T2 (Figs. 7 and 11; and spec. pg. 2, line 23 - pg. 3, line 7; pg. 6, lines 16-19; pg. 10, lines 11-14; pg. 16, line 24 to pg. 17, line 13; pg. 20, lines 6-21; pg. 22, line 28 to pg. 23 line 12; pg. 25, lines 8-14; and original claim 1)
38. A system for sensing RF amplifier output power comprising:	(Fig. 1; pg 1, lines 2-8; and pg. 2, lines 9-14)
a first amplifying transistor device to amplify a RF input signal and generate a RF output signal therefrom;	T1 (Figs. 7 and 11; pg. 6, lines 10-12, pg. 20, lines 6-21)
a second amplifying transistor device to sample a RF input signal that is associated with both the first amplifying transistor device and the second amplifying transistor device and generate a sampled signal therefrom; and	T2 (Figs. 7 and 11; and spec. pg. 2, line 23 - pg. 3, line 7; pg. 6, lines 16-19; pg. 10, lines 11-14; pg. 16, line 24 to pg. 17, line 13; pg. 20, lines 6-21; pg. 22, line 28 to pg. 23 line 12; pg. 25, lines 8-14; and original claim 1)
means for sensing the sampled signal and generating a current sensing signal therefrom proportional to a power amplitude associated with the RF output signal.	Circuitry generates a current (DRAIN (2)) that is proportional to the current of T1 (DRAIN (1)) (Figs. 7 and 11, pg. 16, line 24 to pg. 17, line 9; and pg. 20, lines 6-21)
39. The system of claim 38, wherein said second amplifying transistor device is physically smaller than said first amplifying transistor device.	T2 (Figs. 7 and 11; and spec. pg. 2, line 23 - pg. 3, line 7; pg. 10, lines 11-14; pg. 16, line 24 to pg. 17, line 13; pg. 20, lines 6-21; pg. 22, line 28 to pg. 23 line 12; and original claim 1)
40. The system of claim 39, further comprising biasing means for biasing the second amplifying transistor device and further for biasing the first amplifying transistor device such that a bias current associated with the second amplifying transistor device is proportional to a bias current associated with the first amplifying transistor device.	R1 (Fig. 11) R1 & R2 (Fig. 7) Numerals (4), (5), (8-1)-(8-N) (Fig. 1; pg. 6, lines 4-7 and 23-27; and pg. 20, lines 6-21)

41. A method for sensing RF signal power amplitude, the method comprising the steps of:	(Fig. 1; pg 1, lines 2-8; and pg. 2, lines 9-14)
(a) providing a RF signal amplifier comprising a first transistor having a first predetermined size;	T1 (Figs. 7 and 11; pg. 6, lines 10-12, pg. 20, lines 6-21)
(b) providing a sampling amplifier comprising a second transistor having a second predetermined size that is smaller than the first predetermined size;	T2 (Figs. 7 and 11; and spec. pg. 2, line 23 - pg. 3, line 7; pg. 6, lines 16-19; pg. 10, lines 11-14; pg. 16, line 24 to pg. 17, line 13; pg. 20, lines 6-21; pg. 22, line 28 to pg. 23 line 12; pg. 25, lines 8-14; and original claim 1)
(c) amplifying a RF input signal to produce a first RF output signal; and	T1 (Figs. 7 and 11; pg. 6, lines 10-12, pg. 20, lines 6-21)
(d) sampling the RF input signal to produce a second RF output signal proportional to the first RF output signal, wherein the proportion is associated with a ratio determined by the first and second predetermined sizes.	T2 (Figs. 7 and 11; and spec. pg. 2, line 23 - pg. 3, line 7; pg. 10, lines 11-14; pg. 16, line 24 to pg. 17, line 13; pg. 20, lines 6-21; pg. 22, line 28 to pg. 23 line 12; pg. 25, lines 8-14; and original claim 1)

42. The method of claim 41, further comprising the step of: (e) converting the second RF output signal to a current sensing signal such that the current sensing signal is proportional to a power amplitude associated with the first RF output signal.	Circuitry generates a current (DRAIN (2)) that is proportional to the current of T1 (DRAIN (1)) (Figs. 7 and 11, pg. 16, line 24 to pg. 17, line 9; and pg. 20, lines 6-21)
43. A system for sensing RF amplifier output power comprising:	(Fig. 1; pg 1, lines 2-8; and pg. 2, lines 9-14)
a RF amplifier transistor configured to receive and amplify a RF signal;	T1 (Figs. 7 and 11; pg. 6, lines 10-12, pg. 20, lines 6-21)
a sampling transistor configured to receive and amplify a RF signal, wherein the sampling transistor is physically smaller than the RF amplifier transistor such that the sampling transistor is capable of producing a proportionally smaller amplified RF signal than that capable of being produced by the RF amplifier transistor for a RF input signal common to both the RF amplifier transistor and the sampling transistor;	T2 (Figs. 7 and 11; and spec. pg. 2, line 23 - pg. 3, line 7; pg. 6, lines 16-19; pg. 10, lines 11-14; pg. 16, line 24 to pg. 17, line 13; pg. 20, lines 6-21; pg. 22, line 28 to pg. 23 line 12; pg. 25, lines 8-14; and original claim 1)
a current sensing circuit configured to receive a RF signal amplified by the sampling transistor and generate a current proportional to a power amplitude associated with the RF signal amplified by the RF amplifier transistor; and	Circuitry generates a current (DRAIN (2)) that is proportional to the current of T1 (DRAIN (1)) (Figs. 7 and 11, pg. 16, line 24 to pg. 17, line 9; and pg. 20, lines 6-21)
a bias circuit configured to establish quiescent operating characteristics associated with the RF amplifier transistor and the sampling transistor, the bias circuit comprising a first bias resistor associated with the RF amplifier transistor and further comprising a second bias resistor associated with the sampling transistor.	R1 (Fig. 11) R1 & R2 (Fig. 7) Numerals (4), (5), (8-1)-(8-N) (Fig. 1; pg. 6, lines 4-7 and 23-27; and pg. 20, lines 6-21)

44. Amplifier circuitry comprising:	(Fig. 1; pg 1, lines 2-8; and pg. 2, lines 9-14)
a) a radio frequency power amplifier for amplifying a radio frequency input signal and having: i) a radio frequency amplifier input for receiving the radio frequency input signal, ii) a bias input for receiving a bias signal for biasing the radio frequency power amplifier, and iii) a power amplifier output providing an amplified radio frequency signal;	T1 (Figs. 7 and 11; pg. 6, lines 10-12, pg. 20, lines 6-21)
b) a first transistor circuit having: i) a first input for receiving the radio frequency input signal, ii) a first bias input for receiving the bias signal, and iii) a first output providing a first output signal having a bias component and a radio frequency component proportionally smaller than the amplified radio frequency signal; and	T2 (Figs. 7 and 11; and spec. pg. 2, line 23 - pg. 3, line 7; pg. 6, lines 16-19; pg. 10, lines 11-14; pg. 16, line 24 to pg. 17, line 13; pg. 20, lines 6-21; pg. 22, line 28 to pg. 23 line 12; pg. 25, lines 8-14; and original claim 1)
c) bias circuitry adapted to provide the bias signal as a function of the first output, wherein the bias circuitry provides the bias signal to compensate for output power of the amplified radio frequency signal.	R1 (Fig. 11) R1 & R2 (Fig. 7) Numerals (4), (5), (8-1)-(8-N) (Fig. 1) (pg. 6, lines 4-7 and 23-27; and pg. 20, lines 6-21)
45. The amplifier circuitry of claim 43, wherein the power amplifier circuitry is implemented using transistor circuitry.	T1 (Figs. 7 and 11; pg. 6, lines 10-12, pg. 20, lines 6-21)

46. Amplifier circuitry comprising:	(Fig. 1; pg 1, lines 2-8; and pg. 2, lines 9-14)
a) a radio frequency power amplifier for amplifying a radio frequency input signal and having: i) a radio frequency amplifier input for receiving the radio frequency input signal, ii) a bias input for receiving a bias signal for biasing the radio frequency power amplifier, and iii) a power amplifier output providing an amplified radio frequency signal;	T1 (Figs. 7 and 11; pg. 6, lines 10-12, pg. 20, lines 6-21)
b) a first transistor circuit having: i) a first input for receiving the radio frequency input signal, ii) a first bias input for receiving the bias signal, and iii) a first output providing a first output signal having a bias component and a radio frequency component proportionally smaller than the amplified radio frequency signal; and	T2 (Figs. 7 and 11; and spec. pg. 2, line 23 - pg. 3, line 7; pg. 6, lines 16-19; pg. 10, lines 11-14; pg. 16, line 24 to pg. 17, line 13; pg. 20, lines 6-21; pg. 22, line 28 to pg. 23 line 12; pg. 25, lines 8-14; and original claim 1)
c) bias circuitry adapted to provide the bias signal as a function of the first output, wherein the bias circuitry provides the bias signal based on output power of the amplified radio frequency signal.	R1 (Fig. 11) R1 & R2 (Fig. 7) Numerals (4), (5), (8-1)-(8-N) (Fig. 1; pg. 6, lines 4-7 and 23-27; and pg. 20, lines 6-21)
47. The amplifier circuitry of claim 46, wherein the power amplifier circuitry is implemented using transistor circuitry.	T1 (Figs. 7 and 11; pg. 6, lines 10-12, pg. 20, lines 6-21)

48. A power amplifying circuit comprising:	(Fig. 1; pg 1, lines 2-8; and pg. 2, lines 9-14)
an amplifying transistor which receives an input signal; and	T1 (Figs. 7 and 11; pg. 6, lines 10-12, pg. 20, lines 6-21)
a sense transistor being smaller in size than the output transistor, the sense transistor receiving said input signal,	T2 (Figs. 7 and 11; and spec. pg. 2, line 23 - pg. 3, line 7; pg. 6, lines 16-19; pg. 10, lines 11-14; pg. 16, line 24 to pg. 17, line 13; pg. 20, lines 6-21; pg. 22, line 28 to pg. 23 line 12; pg. 25, lines 8-14; and original claim 1)
wherein an output current of the sense transistor is proportional to an output current of the output transistor.	Circuitry generates a current (DRAIN (2)) that is proportional to the current of T1 (DRAIN (1)) (Figs. 7 and 11, pg. 16, line 24 to pg. 17, line 9; and pg. 20, lines 6-21)
49. A power amplifying circuit comprising:	(Fig. 1; pg 1, lines 2-8; and pg. 2, lines 9-14)
a first transistor which receives an input signal and generates an output;	T1 (Figs. 7 and 11; pg. 6, lines 10-12, pg. 20, lines 6-21)
a second transistor being smaller in size than the first transistor, the second transistor also receiving said input signal; and	T2 (Figs. 7 and 11; and spec. pg. 2, line 23 - pg. 3, line 7; pg. 6, lines 16-19; pg. 10, lines 11-14; pg. 16, line 24 to pg. 17, line 13; pg. 20, lines 6-21; pg. 22, line 28 to pg. 23 line 12; pg. 25, lines 8-14; and original claim 1)
a resistor element coupled to the second transistor, wherein a voltage formed across the resistor element is proportional to the output of the first transistor.	Rs1, (Fig. 11; pg. 2, line 27 - pg. 3, line 5; pg. 16 lines 11-14; pg. 17, lines 5-9; pg. 20, lines 15-21) Rs. (Fig. 7)